Chapter 7 The CPU And Memory

1) The Little Man instruction set is based on a decimal number system; real computers encode instructions and data using the

a) binary system.

b) Unicode system.

c) decimal system.

d) algebraic system.

2) The ALU and CU together are known as the

a) CPU.

b) instruction set.

c) program counter.

d) Memory Management Unit.

3) The area inside of the CPU that holds data temporarily and performs calculations is called the

a) accumulator.

b) program counter.

c) arithmetic logic unit.

d) Memory Management Unit.

4) The storage locations that are used for a particular defined purpose within the CPU are called

a) RAM.

b) storage.

c) the bus.

d) registers.

5) The 1-bit registers that are used to allow the computer to keep track of special conditions (like overflow or power failure) are often called

a) flags.

b) loops.

c) the ALU.

d) I/O counters.

6) Loading the value zero into a register is called

a) inverting a register.

b) clearing a register.

c) dumping the register.

d) incrementing a register.

7) The register that holds the address of the memory location that needs to be accessed is called the

a) IR.

b) MAR.

c) MDR.

d) MBR.

8) The register that holds the current instruction is called the

a) IR.

b) PC.

c) LMC.

d) MBR.

9) The register that will hold the data value that is being transferred between the CPU and a particular memory location is called the

a) PC.

b) ALU.

c) MAR.

d) MDR.

10) The mailboxes in the LMC model are the equivalent to a real computer's

a) CPU.

b) ports.

c) memory.

d) control unit.

11) Which of the following is NOT one of the three lines that control the memory cell?

a) Skew line

b) Address line

c) Read/write line

d) Activation line

12) If the Memory address register is 8 bits wide, the number of possible memory addresses is

a) 8

b) 16

c) 64

d) 256

13) Memory that retains its values when power is removed is called

a) DRAM.

b) SRAM.

c) volatile.

d) nonvolatile.

14) There would never be a reason for an address transfer from the \_\_\_\_\_\_\_\_ to another register within the CPU.

a) IR

b) PC

c) MAR

d) MDR

15) When the instruction being executed is to store data, the data will be transferred from another register in the CPU to the \_\_\_\_\_, and from there it will be transferred into memory.

a) IR

b) PC

c) MAR

d) MDR

16) The different ways of establishing memory addresses within an instruction are called

a) MAR codes.

b) MDR codes.

c) addressing modes.

d) programmable modes.

17) Flash Memory

a) is volatile.

b) is faster than standard RAM.

c) has unlimited rewrite capacity.

d) is nonvolatile.

18) The first step in the instruction cycle is

a) clear the accumulator.

b) fetch the instruction from memory.

c) decode the instruction in the accumulator.

d) copy the data from the MAR to the MDR.

19) The physical connections that make it possible to transfer data from one location in the computer system to another are called

a) flags.

b) fibers.

c) buses.

d) peripherals.

20) Optical conductors are

a) faster than electrical conductors.

b) cheaper than electrical conductors.

c) more common than electrical conductors.

d) all of the above.

21) A bus in which there is an individual line for each bit of data, address, and control is called a

a) wide bus.

b) serial bus.

c) parallel bus.

d) dedicated bus.

22) A bus that transfers data sequentially, one bit at a time using just a single line pair is called

a) a serial bus.

b) a single bus.

c) a narrow bus.

d) a sequential bus.

23) A bus line that is "one-way" is called

a) a simplex bus line.

b) a serial bus line.

c) a one-way bus line.

d) a sequential bus line.

24) A bus line that can carry data in both directions at the same time is called a

a) simplex bus line.

b) complex bus line.

c) full duplex bus line.

d) half duplex bus line.

25) The exposed connectors into which external cables can be plugged are often called

a) plugs.

b) lines.

c) ports.

d) stacks.

26) A bus that carries signals from a single specific source to a single specific destination is a(n)

a) simplex bus.

b) broadcast bus.

c) Ethernet bus.

d) point-to-point bus.

27) Virtually every bus internal to the CPU is

a) serial.

b) cables.

c) optical.

d) parallel.

28) Instructions that only the operating system can execute are called

a) system instructions.

b) executive instructions.

c) privileged instructions.

d) administrative instructions.

29) Programs that execute without privileges are said to execute

a) in user space.

b) in data mode.

c) in kernel space.

d) in privilege space.

30) Multimedia applications, like modifying an image, often use

a) PSW instructions.

b) Flash instructions.

c) MMD instructions.

d) SIMD instructions.

31) The sources and destinations of data for an instruction are known as

a) Op codes.

b) Operands.

c) Op registers.

d) Operation fields.

32) Increasing the number of bits available for the op code in an instruction word

a) increases the demand on the CPU.

b) increases the number of memory locations that can be addressed.

c) increases the number of instructions available in the instruction set.

d) has no impact on any of the above.

Discussion Questions

1) How are the registers in the CPU different from main memory?

Sol: From the text: “A register is a single, permanent storage location within the CPU used for a particular, defined purpose. A register is used to hold a binary value temporarily for storage, for manipulation, and/or for simple calculations. Note that each register is wired within the CPU to perform its specific role. That is, unlike [main] memory, where every address is just like every other address, each register serves a particular purpose. The register's size, the way it is wired, and even the operations that take place in the register reflect the specific function that the register performs in the computer.” Alternately: Register access is much faster, and there are far fewer registers than memory locations.

2) How does the computer keep track of special conditions such as arithmetic carry and overflow, power failure, and internal computer error?

Sol: From the text “The control unit will also contain several 1-bit registers, sometimes known as flags, that are used to allow the computer to keep track of special conditions such as arithmetic carry and overflow, power failure, and internal computer error. Usually, several flags are grouped into one or more status registers.”

3) What factor factor determines the maximum capacity of memory in a real computer?

Sol: The number of bits in the memory address register determines the maximum number of memory locations that can be addressed.

4) Why is it necessary to store start-up program code in nonvolatile memory?

Sol: from the text “At least some of the program code used to start a computer must be present in a nonvolatile segment of primary memory. (Otherwise there would be no program in memory to execute when the computer is powered up!) This code is known as firmware.”

5) Why is flash memory not suitable for use as main memory?

Sol: from the text “[Flash memory] is generally considered unsuitable for primary memory because it is not possible to write to a single memory location. Instead it is necessary to erase and rewrite a large block of memory to make any changes in flash memory. The rewrite time is extremely slow compared to standard RAM and the number of rewrites over the lifetime of flash memory is somewhat limited.”

6) Classify the registers as either a) holding addresses only, b) holding instructions only, or c) anything.

IR \_\_\_\_

PC \_\_\_\_

MAR \_\_\_\_

MDR \_\_\_\_

Accumulator \_\_\_\_

General Purpose \_\_\_\_

Sol:

IR (b) holding instructions only

PC (a) holding addresses only

MAR (a) holding addresses only

MDR (c) anything

Accumulator (c) anything

General Purpose (c) anything

7) What is the technique that real computers use to extend the address space beyond that of the address field in an instruction?

Sol: From the text “…….one common method, consider a computer that can use one of the general-purpose registers to hold an address. To find a memory location, the computer would use the value in that register as a pointer to the address. Instead of an address field, the instruction needs only to indicate which register contains the address. Using this technique, the addressing capability of the computer is determined by the size of the register.”

8) What is skew?

Sol: The slight delay in arrival time on different lines as signals traverses a parallel bus.

9) What are “Arithmetic Shifts” commonly used for?

Sol: from the text “Arithmetic shift instructions are commonly used to multiply or divide the original value by a power of 2.”

10) Explain *pop* and *push* operations on a stack.

Sol: A pop is when data comes off the stack and a push is when data is put in the stack. Stacks are used to implement last-in, first-out structures.

11) Why are input/output instructions generally considered privileged instructions?

Sol: from the text: “Input/output instructions are generally privileged instructions because we do not want input and output requests from different users and programs interfering with each other.”

To avoid interference, the OS handles the I/O requests.

12) What are different ways of characterizing a bus? In other words, what attributes do all buses have?

Sol: From the text “A bus can be characterized by the number of separate wires or optical conductors in the bus; by its throughput, that is, the data transfer rate measured in bits per second; by the data width (in bits) of the data being carried; by the number and type of attachments that the bus can support; by the distance between the two end points; by the type of control required; by the defined purpose of the bus; by the addressing capacity; by whether the lines on the bus are uniquely defined for a single type of signal or shared; and by the various features and capabilities that the bus provides.”

13) Why is there no need for a *subtract* instruction?

Sol: Subtracting a number from another number is the same as changing the sign of the subtrahend and adding. That is, 5-9 is the same as 5+(-9).

From the text: “Even the subtract instruction is theoretically not necessary, since we showed in Chapter 5 that integer subtraction is performed internally by the process of complementing and adding.”

14) Identify the implicit and explicit addresses in the Little Man instruction 531; recall that “5” is the op code for the load instruction.

Sol: The instruction 531 is a load from mailbox 31 to the accumulator. The explicit address is 31 and the accumulator is the implicit address.

15) What is an important disadvantage of variable length instructions?

Sol: From the text: “Variable length instructions complicate pipelining, because the starting point of the new instruction is not known until the length of the previous instruction has been determined. If you extend this idea to multiple instructions, you can see the difficulty of maintaining a smooth assembly line. This issue is discussed in more detail in Chapter 8. Because pipelining has become so important to processing speed in modern computers, the use of variable length instructions has fallen out of favor for new CPU designs. Nearly all new CPU designs use fixed length instructions exclusively.”

|  |  |  |
| --- | --- | --- |
| Problem | Answer | Section in text / comments |
| 1 | a | Section 7.0 Introduction |
| 2 | a | Section 7.1 The Components of the CPU |
| 3 | c | Section 7.1 The Components of the CPU |
| 4 | d | Section 7.2 The Concept of Registers |
| 5 | a | Section 7.2 The Concept of Registers |
| 6 | b | Section 7.2 The Concept of Registers |
| 7 | b | Section 7.2 The Concept of Registers |
| 8 | a | Section 7.2 The Concept of Registers |
| 9 | d | Section 7.2 The Concept of Registers |
| 10 | c | Section 7.3 The Memory Unit |
| 11 | a | Section 7.3 The Memory Unit |
| 12 | d | Section 7.3 The Memory Unit |
| 13 | d | Section 7.3 The Memory Unit |
| 14 | c | Section 7.3 The Memory Unit |
| 15 | d | Section 7.3 The Memory Unit |
| 16 | c | Section 7.3 The Memory Unit |
| 17 | d | Section 7.3 The Memory Unit |
| 18 | b | Section 7.4 The Fetch-execute  |
| 19 | c | Section 7.5 Buses |
| 20 | a | Section 7.5 Buses |
| 21 | c | Section 7.5 Buses |
| 22 | a | Section 7.5 Buses |
| 23 | a | Section 7.5 Buses |
| 24 | c | Section 7.5 Buses |
| 25 | c | Section 7.5 Buses |
| 26 | d | Section 7.5 Buses |
| 27 | d | Section 7.5 Buses |
| 28 | c | Section 7.6 Classification of Instructions |
| 29 | a | Section 7.6 Classification of Instructions |
| 30 | d | Section 7.6 Classification of Instructions |
| 31 | b | Section 7.7 Instruction Word Formats |
| 32 | c | Section 7.8 Instruction Word Requirements and Constraints |