Assignment 1

Q. [1] The work performed by an individual computer system within the IT system can be characterized by the Input-Process-Output (IPO) model. Use the IPO model to analyze the process of purchasing a soft drink from a vending machine. Keep it simple!

(More sophisticated responses could appear; here is a simplistic model) INPUT: Money in the form of paper bills or coins; drink selection PROCESSING: Check the integrity of the money; calculate the change; OUTPUT: dispense the change and drink

Q. [2] What is the top-down approach to system architecture?

Short description: Start with the system as a whole and then continuously decompose each function into a set of dependent subsystems of increasing detail.

Sol: from the text: "The analysis, design, and implementation of IT systems must take place at different levels of detail and frequently require collaboration among many analysts and designers. This corresponds well with the ability to decompose systems into components, hierarchically, which allows us to concentrate at the appropriate levels of detail during each step along the way. This approach is known as a top-down approach."

Q. [3] Give a short description of peer-to-peer architecture.

Sol: from the text: "An alternative to client-server architecture is peer-to-peer architecture. Peer- to-peer architecture treats the computers in a network as equals, with the ability to share files

Sol: (More sophisticated responses could appear; here is a simplistic model) INPUT: Money in the form of paper bills or coins; drink selection PROCESSING: Check the integrity of the money; calculate the change; OUTPUT: dispense the change and drink
and other resources and to move them between computers."

Q. [4] Explain 5 simple data types in detail.

Boolean:
Character:
Enumerated:
Integer and real:

Q. [5] What is COLLATING SEQUENCE?

A collating sequence (also called a sort sequence) defines how characters in a character set relate to each other when they are compared and ordered. ... SBCS character data (including bit data) the SBCS portion of mixed data. Unicode data (UTF-8, UCS-2, or UTF-16).
Alphabetic sorting if software handles mixed upper- and lowercase codes. In ASCII, numbers collate first; in EBCDIC, last. ASCII collating sequence for string of characters.

Q. [6] Explain ASCII, EBCEDIC & UNICODE with examples.

ASCII - most widely used coding scheme
EBCDIC: IBM mainframe (legacy)
Unicode: developed for worldwide use

Q. [7] List five specific skills or abilities required of an information technology (IT) systems architect or system analyst?

Any five from the following
In systems design, the architects are responsible for:
Interfacing with the user(s) and sponsor(s) and all other stakeholders in order to determine their (evolving) needs.
Generating the highest level of system requirements, based on the user's needs and other constraints.
Ensuring that this set of high level requirements is consistent, complete, correct, and operationally defined.
Performing cost–benefit analyses to determine whether requirements are best met by manual, software, or hardware functions; making maximum use of commercial off-the-shelf or already developed components.
Developing partitioning algorithms (and other processes) to allocate all present and foreseeable requirements into discrete partitions such that a minimum of communications is needed among partitions, and between the user and the system.
Partitioning large systems into (successive layers of) subsystems and components each of which can be handled by a single engineer or team of engineers or subordinate architect.
Interfacing with the design and implementation engineers and architects, so that any problems arising during design or implementation can be resolved in accordance with the fundamental design concepts, and user needs and constraints.
Ensuring that a maximally robust design is developed.

Generating a set of acceptance test requirements, together with the designers, test engineers, and the user, which determine that all of the high level requirements have been met, especially for the computer-human-interface.
Generating products such as sketches, models, an early user guide, and prototypes to keep the user and the engineers constantly up to date and in agreement on the system to be provided as it is evolving.
Ensuring that all architectural products and products with architectural input are maintained in the most current state and never allowed to become obsolete.

A systems analyst may:
Identify, understand and plan for organizational and human impacts of planned systems, and ensure that new technical requirements are properly integrated with existing processes and skill sets.
Plan a system flow from the ground up.
Interact with internal users and customers to learn and document requirements that are then used to produce business requirements documents.
Write technical requirements from a critical phase.
Interact with designers to understand software limitations.
Help programmers during system development, e.g. provide use cases, flowcharts or even database design.
Perform system testing.
Deploy the completed system.
Document requirements or contribute to user manuals.
Whenever a development process is conducted, the system analyst is responsible for designing components and providing that information to the developer.

Q. [8] Perform the following conversion, demonstrate all the steps:

(3D70)16 to (15728)10

3 x 163 + 13 x 162 + 7 x 16 + 0 = 15728

(11101)2 to (29)10

1x24 + 1x23 + 1x22 + 0 + 1 = 29

(110001100011001)2 to (6319)16

1001 = 9

0001 = 1

0011 = 3

1100 = 6

(624)8 to (404)10

6 x 82 + 2 x 8 + 4 =404

Assignment 2

Question No.1: Define the terms assembler and compiler in one line**.**

Assembler translate assembly language into machine code and compiler translate high level language to machine code

Question No.2: For LMC, write assembly code to add two numbers and then subtract a third number (the subtraction answer should be positive)

Mailbox	Mnemonic	Instruction Description
00	IN	input 1st Number
01	STO 98	store data
02	IN	Input 2nd Number
03	ADD 98	add 1st Number to 2nd
04	STO 98	store sum
05	IN	input 3rd Number
06	STO 99	store data
07	SUB 98	subtract data in 99 from calculator
08	BRP 11	Positive
09	LDA 98	Negative
10	SUB 99	subtract data in 99 from calculator
11	OUT	output result
12	COB	Stop
98	DAT 00	data
99	DAT 00	data

Question No.3: Find the 9's complementary representation.

a) What is the sign-and-magnitude value of the three-digit number represented in 9's complement by 367?

a) In 9's complement, numbers 0 to 499 are positive, hence 367 is +367.

b) What is the sign-and-magnitude value of the three-digit number represented in 9's complement by 840?

b) In 9's complement, numbers 500 to 998 are negative, so we find the complement:

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 999
-840
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 159
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Adjust sign: answer is -159

Note:

To solve the following problems, Use the Floating point format SEEMMMMM, where

(a) S = 0 is "+" and 5 is "-"

(b) EE is the exponent in excess-50 notation, and

(c) MMMMM are five digits of mantissa.

Question No.4: Show how 12.25 is represented in SEEMMMMM format?

$12.25 = .1225 \times 10^2$
S=0
EE=52
MMMMM = 12250, where the added zero is added to make five digits

Answer: 05212250

Question No. 5: Add the two floating point numbers 04933460 and 04877456 (in SEEMMMMM format.)

Given two numbers can be look like:
04933460 ---> $+.33460 \times 10^{-1}$ or 0.033460

04877456 ---> $+.77456 \times 10^{-2}$ or 0.0077456

Now, To add two floating point numbers:
04933460
+
04877456
———————

Step-1: Align Exponents

04933460
+
049077456
———————

Step-2: Add Mantissas

33460 + 077456 = 412056
After addition, it look like, 04941206(6)
Step-3: Round the result
04941207

Answer is: 04941207 -> $+.41207 \times 10^{-1}$

Assignment 3

Question No. 1: Explain any three important instruction set design issues.

Operation repertoire: How many and which operations to provide, and how complex operations should be

Instruction format: Instruction length, number of addresses and size of various fields

Registers: Number of processor registers that can be referenced by instructions, and their use

Data types: The various types of data upon which operations are performed

Addressing: The mode or modes by which the address of an operand is specified

Question No. 2: Is it easier to write programs in assembly codes using CISC compared to RISC? Why?

Yes, because CISC instructions are complex and designed to do more than one task in one instruction. This would reduce the amount of instructions needed to code a program.

Question No. 3: Which instructions can reference memory in CISC and RISC?

In RISC, only LOAD and STORE instructions can reference memory.

In CISC, all instructions can reference memory.

Question No. 4: How do you translate the high-level statement : C=A+B into instructions:

Using 3 addresses instructions format

Using 2 addresses instructions format

Assume A, B, C are CPU registers and the following mnemonics exist: ADD, SUB, MOVE

3 addresses	2 addresses
ADD C,A,B	MOVE C,A ADD C,B

Question No. 5: What is the benefit of pipelining? And how it works?

It is a technique that allows for simultaneous execution of parts, or stages, of instructions to more efficiently process instructions. It works by dividing instructions into 4 stages: fetch, decode, execute and write-back and executing multiple stages of different instruction each clock cycle.

Question No. 6: What are the basic elements of a machine instruction?

Operation code

Source operand reference

Result operand reference

Next instruction reference

Question No. 7: Define the following:

a) Fetch – Execute Cycle

Fetch

Decode or find instruction, load from memory into register and signal ALU

Execute

Performs operation that instruction requires

Move/transform data

b) MAR – MDR

Memory Address Register (MAR)

Memory Data Register (MDR)

c) Status Register

Status of CPU and currently executing program

Flags (one bit Boolean variable) to track condition like arithmetic carry and overflow, power failure, internal computer error

Assignment 4

Q1: What are the three techniques to improve performance of CPU?

- Separating the fetch-execute cycle into two separate fetch and execute units that can operate in parallel
- Pipelining to allow instructions to execute in an assembly line
- Multiple execution units to allow parallel execution of unrelated instructions

Q2: Describe how a *cache memory* is organized?

Cache memory is organized into blocks. Each block provides a small amount of storage, perhaps between 8 and 64 bytes, also known as a **cache line.** Each block also holds a **tag,** a pointer to location in main memory. A hardware **cache controller** checks the tags to determine if the memory location of the request is presently stored within the cache. The ratio of hits to the total number of requests is known as the **hit ratio**. Synchronizing cache and memory, Write through and write back.

Q3: What are the three different approaches are commonly used to enhance the performance of memory?

- Wide path memory access
- Memory interleaving
- Cache memory

Q4: Narrate about Direct Memory Access (DMA)?

- Transferring large blocks of data
- Direct transfer to and from memory
- CPU not actively involved in transfer itself
- Required conditions for DMA
    - The I/O interface and memory must be connected
    - The I/O module must be capable of reading and writing to memory
    - Conflicts between the CPU and the I/O module must be avoided
    - Interrupt required for completion

Q5: Write different I/O module functions in computer?

- Recognizes messages from device(s) addressed to it and accepts commands from the CPU
- Provides a buffer where the data from memory can be held until it can be transferred to the device
- Provides the necessary registers and controls to perform a direct memory transfer
- Physically controls the device
- Copies data from its buffer to the device/from the CPU to its buffer
- Communicates with CPU

Q6: Describe the difference between active matrix display and passive matrix display in a liquid crystal display (LCD) monitor. Which results in a brighter picture?

From the text: "In an active matrix display, the display panel contains one transistor for each cell in the matrix. This guarantees that each cell will receive a strong charge, but is also expensive and difficult to manufacture." In a passive matrix display, a single transistor is used for each row and column of the matrix and activates each cell, one at a time, repetitively, using a scan pattern. The active matrix display is brighter.

Q7: Explain Constant Angular Velocity (CAV) and Constant Linear Velocity (CLV)?

Constant Angular Velocity

- Number of bits on each track is the same! Denser towards the center.
- Spins the same speed for every track

Constant Linear Velocity

- All tracks have the same physical length and number of bits
- Constant speed reading data off a track

Drive has to speed up when accessing close to the center of the drive and slow down when accessing towards the edge of the drive

Q8: Explain how a mirrored array, consisting of 4 disk drives, would be approximately 4 times faster during a multiblock read?

In a mirrored array, each disk stores exactly the same data. During reads, alternate blocks of the data are read from different drives, then combined to reassemble the original data. Thus, the access time for a multiblock read is reduced approximately by a factor equal to the number of disk drives in the array.

Assignment 5

Q1. What are the advantages of Client-Server Architecture?

- Centralization of services permits
  - easier administration of services by IT professionals
  - easier availability and location by users
  - consistency of resources, such as files and data, can be managed and assured
  - more efficient and cost-effective hardware procurement through purchasing a small number of very powerful computers

Q2. Differentiate between Bitmap vs. Object Images.

Bitmap (Raster)	**Object (Vector)**
Pixel map	Geometrically defined shapes
Photographic quality	Complex drawings
Paint software	Drawing software
Larger storage requirements	Higher computational requirements
Enlarging images produces jagged edges	Objects scale smoothly
Resolution of output limited by resolution of image	Resolution of output limited by output device

Q3. Explain GIF (Graphics Interchange Format) and JPEG (Joint Photographers Expert Group)

GIF (Graphics Interchange Format):

- First developed by CompuServe in 1987
- GIF89a enabled animated images
  - allows images to be displayed sequentially at fixed time sequences
- Color limitation: 256
- Image compressed by LZW (Lempel-Zif-Welch) algorithm
- Preferred for line drawings, clip art and pictures with large blocks of solid color
- *Lossless compression*

JPEG (Joint Photographers Expert Group):

- Allows more than 16 million colors
- Suitable for highly detailed photographs and paintings
- Employs *lossy compression* algorithm that
  - Discards data to decreases file size and transmission speed
  - May reduce image resolution, tends to distort sharp lines

Q4 (a) . Perform the following conversion, demonstrate all the steps: (0.5)

a. $(101011010)_2$ to ($)_{10}$
b. $(101011010)_2$ to ($)_{16}$
c. $(5D3)_{16}$ to ($)_2$
d. $(1234)_8$ to ($)_{10}$

a. $(101011010)_2 = 1x2^8 + 0x2^7 + 1x2^6 + 0x2^5 + 1x2^4+1x2^3+ 0x2^2 + 1x2^1+ 0x2^0 = 346$

b. $(1\ 0101\ 1010)_2= 15A$

c. $(5D3)_{16} = 10111010011$

d. $(1234)_8 = 1x8^3 + 2x8^2 + 3x8 + 4 = 668$

(b) Given -0.35645*10-6, what is the mantissa, sign of mantissa and exponent in the expression?

mantissa: 35645, sign of mantissa: - (minus), exponent: 6

Q.5 Define a bus? Differentiate between point-to-point bus and multipoint bus.

Bus:The physical connection that makes it possible to transfer data from one location in the computer system to another

Point-to-point: a bus that carries signals from single source to specified single destination is identified as point-to-point bus.

Multipoint bus: a bus used to connect several points together is called multipoint bus

Q.6 Write the role of MAR and MDR?

MAR: Memory address register. It holds the address of a memory location

MDR: Memory data register. Holds the data value that is being stored to or retrieved from the memory location currently addressed by the memory address register

Q.7 What are the four primary operations that are normally performed on registers?

Stores values from other locations (registers and memory)

Addition and subtraction

Shift or rotate data

Test contents for conditions such as zero or positive

Q.8 What is the function of registers in the fetch-execute instruction cycle? What is the purpose of the instruction register?

A register is used to hold a binary value temporarily for storage, for manipulation, and/or for simple calculations.

A register may hold data being processed, an instruction being executed, a memory or I/O address to be accessed, or even special binary codes.

Instruction Register (IR) Stores instruction fetched from memory

Q.9 Define the terms:

- Master slave multiprocessing
- Symmetrical multiprocessing

Master-slave multiprocessing, in which one CPU, the master, manages the system, and controls all resources and scheduling. Only the master may execute the operating system. Other CPUs are slaves, performing work assigned to them by the master.
Symmetrical multiprocessing (SMP): in which each CPU has identical access to the operating system, and to all system resources, including memory. Each
CPU schedules it own work, within parameters, constraints, and priorities set by the operating system in a normal SMP configuration, each of the CPUs is Identical.

Q.10 Represent the value (-45)10 in binary using

a. Signed magnitude
b. 1's complement
c. 2's complement

signed magnitude: -45 is 10101101

1's complement: Flip 10101101 → 11010010

2's complement: 1's complement + 1 → 11010010+1 → 11010011

Q.11 Discuss how writing a device driver for a hard disk would require an in-depth understanding of how the hardware functions. Would you also need an in-depth understanding of the OS platform for which the device was designed to function?

I/O controllers work at the CPU interface and the device interface. The I/O device controller must understand the specific OS instructions for CPU interfacing tasks: accepting I/O commands from the CPU, transferring data between the controller and the CPU or memory, and sending interrupts and status information to the CPU. At the device interface, the I/O controller must be able to control the device, such as moving the mechanical read/write head to the correct track in a disk drive, when to read or write data on the track, and maintaining rotational speed of the disk. Thus, writing a device driver would require an in-depth understanding of the OS and hardware.

Q.12 Explain what is meant by wear-leveling in Flash drives?

Wear-leveling is a technique that is designed to extend the life of a flash memory device. Most failures in flash memory result from erase operations. Furthermore, from the text: control logic, within the flash memory chip, manages memory space allocation and attempts to distribute the write operations evenly over the entire space to minimize the number of erasures required.

Q.13 If three mirrored drives are used in a fault-tolerant system, describe how majority logic is used to decide if the integrity of the data is usable.

If the data from all three disks is identical, then it is safe to assume that the integrity of the data is acceptable. If the data from one disk differs from the other two, then the majority data is used, and the third disk is flagged as an error.

Q.14 Compare and contrast the different disk layouts.

CAV	CLV
Number of bits on each track is the same! Denser towards the center.	All tracks have the same physical length and number of bits
Spins the same speed for every track	Constant speed reading data off a track
CAV discs can store up to 30 minutes per side.	CLV discs can store up to 1 hour per side
Transfer rate is variable	Spindle speed is kept constant while the write speed constantly changes.
It has the advantage of simplicity and fast access.	The design of CLV makes it more difficult to access individual blocks of data rapidly.
Translation speed 50 µ/s	Translation speed 48 – 20 µ/s
Faster and newer CD-ROM drives, hard disk drives, floppy disk drives	Conventional CD-ROM drives